REMARKS

The following remarks are fully and completely responsive to the Office Action dated July 26, 2005. Claims 3, 6, 9 and 11-15 are pending in this application. In the outstanding Office Action, claims 3, 6, 9 and 11-15 were rejected under 35 U.S.C. § 103(a) (three different rejections). No new matter has been added. Claims 3, 6, 9 and 11-15 are presented for reconsideration.

35 U.S.C. § 103(a)

Claims 11-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,349,366, "Yamazaki") in view of Dawson et al. (U.S. Patent No. 6,229,506, "Dawson"). In making this rejection, the Office Action asserts that the combination of the references teaches and/or suggests the claimed invention. The Office Action also asserts that a person of ordinary skill in the art would combine these two references. Applicants respectfully disagree and request reconsideration of this rejection.

Claims 3, 6 and 9 (Office Action mistakenly included claim 15, which depends on claim 14) were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Dawson and further in view of Black et al. (U.S. Patent No. 6,069,381, "Black"). In making this rejection, the Office Action asserts that the combination of these three references teaches and/or suggests the claimed invention. The Office Action also asserts that a person of ordinary skill in the art would combine these three references. Applicants respectfully disagree and request reconsideration of this rejection.

Independent claim 6 recites in part:

> ...a capacitor connected between said second metal layer and a ground or a write line,
>
> wherein the control data is written to said MFMIS structure transistor by using said control line and said ground or said write line.

Claim 11 recites in part:

> ...a capacitor connected between said gate and a ground or a write line,
>
> wherein the control data is written to said ferroelectric capacitor by using said control line and said ground or said write line.

The Office Action admits that Yamazaki fails to teach and/or suggest a capacitor connected between a gate and a ground or a write line. The Office Action cites Dawson as correcting this deficiency in Yamazaki.

The Office Action asserts that Dawson teaches a capacitor (450) connected between a gate (G of P1) and a write line (420). See the Office Action, page 2, section 3.

In contrast, Dawson actually teaches in Fig. 4 and column 5, lines 38-50, a capacitor 450 that is connected to gate G of transistor P1. Capacitor 450 is also connected to data line 410 through transistor P4. Transistor P4 is turned on/off by a signal from select line 420.

Consequently, Dawson fails to teach that capacitor 450 is connected between the second metal layer and a ground or a write line as recited in claim 6 or between the gate and a ground or write line as recited in claim 11. Therefore, Dawson fails to correct the deficiency identified by the Office Action in Yamazaki.

Black is neither cited for nor corrects this deficiency in Yamazaki.

Accordingly, neither the combination of Yamazaki and Dawson nor the combination of Yamazaki, Dawson and Black teach and/or suggest the claimed invention. Regarding claim 6 and the claims dependent thereon, the combination of the cited prior art fails to teach and/or suggest the recited MFMIS structure and a capacitor connected between the second metal layer and a ground or write line. Regarding claim 11 and the claims dependent thereon, the cited prior art fails to teach and/or suggest a ferroelectric capacitor connected between a gate of said MOS transistor and a control line, and a capacitor connected between the gate and a ground or write line. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 3, 6, 9 and 11-13 under 35 U.S.C. § 103(a) (two different rejections).

Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Black and further in view of Hidaka et al. (U.S. Patent No. 6,521,927, "Hidaka"). In making this rejection, the Office Action asserts that the combination of these three references teaches and/or suggests the claimed invention. The Office Action also asserts that it would be obvious to one of ordinary skill in the art to combine these three references. Applicants respectfully disagree and request reconsideration of this rejection.

Independent claim 14 recites in part:

> ...wherein said nonvolatile data holding section is constituted by an element utilizing a magnetoresistance effect or a single electron memory.

The Office Action, on page 4, asserts that Hidaka teaches utilizing a single electron memory at column 1, lines 18-24. This section recites:

> a ferroelectric memory (FRAM) comprising an array of memory cells each using an ferroelectric film as the capacitor insulation film or in a dynamic random access memory (DRAM) comprising an array of dynamic memory cells each using an ferromagnetic film as the capacitor insulator film.
>
> Recently, attention is being drawn to a non-volatile ferroelectric memory cells (FRAM cells) using, as the interelectrode insulation films, ferroelectric films composed of a material the perofskite structure or the lamellar perofskite structure and also to FRAM including an array consisting of the cells.

Hidaka, column 1, lines 16-28.

While Hidaka discusses a ferroelectric memory and using a ferroelectric film, Hidaka fails to disclose and/or suggest a single electron memory.

A single electron memory is a structure in which electrons are stored in quantum dot over a barrier region (tunnel insulator film). This structure is different from a DRAM.

Additionally, the DRAM is a nonvolatile memory element that cannot serve as a nonvolatile data holding section.

Consequently, the combination of these three references fails to teach and/or suggest the claimed invention. Specifically, the combination of these three references fails to teach and/or suggest that the nonvolatile data holding section is constituted by an element utilizing a magnetoresistance effect or a single electron memory. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 14 and 15 under 35 U.S.C. § 103(a).

Conclusion

Applicants' remarks have overcome the rejections set forth in the Office Action dated July 26, 2005. Specifically, Applicants' remarks have distinguished claims 11-13 from the combination of Yamazaki and Dawson and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants' remarks have distinguished claims 3, 6 and 9 from the combination of Yamazaki, Dawson and Black and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants' remarks have distinguished claims 14 and 15 from the combination of Yamazaki, Black and Hidaka and thus overcome the rejection of this claim under 35 U.S.C. § 103(a). Accordingly, claims 3, 6, 9 and 11-15 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 3, 6, 9 and 11-15.

Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 107400-00021.

Respectfully submitted,
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